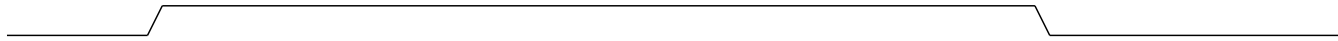




CLK\_SYS



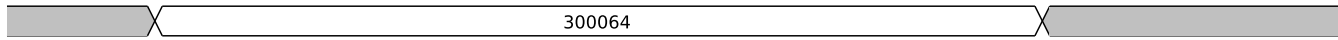
SCS



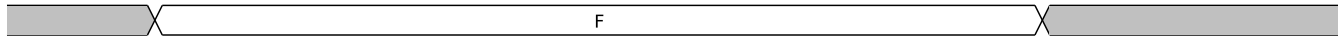
SRD



ADD[23:0]



SBE[3:0]



DATA\_OUT[31:0]

